

Packet No. 9793822-4032

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re U.S. Patent Application of:  
Ohsawa *et al.*

Serial No.: 09/199,305

Filed: November 25, 1998

For: **A SEMICONDUCTOR DEVICE AND  
AN ELECTRICAL DEVICE USING  
THE SEMICONDUCTOR DEVICE**

Examiner: L. Thai

Group Art Unit: 2811

26/ Appeal  
Brief  
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8/27/02  
JUL 29 2002  
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**APPELLANT'S MAIN BRIEF ON APPEAL**

Assistant Commissioner for Patents  
Washington D.C. 20231

Sir:

Appellant is submitting herewith, in triplicate, Appellant's Main Brief on Appeal under 37 C.F.R. §1.192 in support of the Notice of Appeal filed on February 11, 2002.

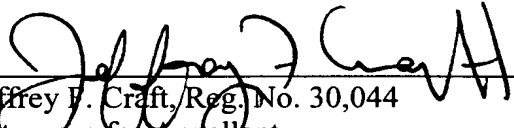
The Commissioner is hereby authorized to charge any fee due not paid by check and to credit any overpayment in fees associated with this communication to Deposit Account No. 19-3140. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

SONNENSCHN NATH & ROSENTHAL

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Jeffrey F. Craft, Reg. No. 30,044  
Attorneys for Appellant

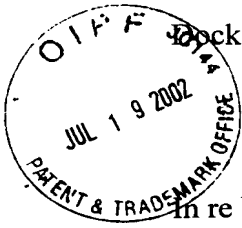
I hereby certify that this original and two copies of this correspondence and any fee being referred to as attached or enclosed is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231 on July 11, 2002.

July 11, 2002  
Date

  
Kathleen Gaines

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PATENT



Docket No. 9793822-4032

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re U.S. Patent Application of:  
Ohsawa *et al.*

Serial No.: 09/199,305

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Assistant Commissioner for Patents  
Washington D.C. 20231  
Sir:

In accordance with the provisions of 37 C.F.R. §1.192, Appellant herewith submits this Brief in support of the Appeal of the above-referenced application.

**REAL PARTY IN INTEREST:**

Sony Corporation, a Japanese corporation with offices at 7-35 Kitashinagawa 6-Chome, Shinagawa-Ku, Tokyo, Japan is the real party in interest.

**RELATED APPEALS AND INTERFERENCES:**

Neither Appellant, Appellant's legal representative, or its assignees are aware of any other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**STATUS OF CLAIMS:**

Claims 1-13 were present in the original application. Claims 6-10 were cancelled in response to a restriction requirement. Claims 14 and 15 were added by amendment. Appellant appeals final rejection of claims 1-5 and 11-15.

## STATUS OF AMENDMENTS:

No amendments were filed subsequent to final rejection

## SUMMARY OF THE INVENTION:

Appellant has discovered improved semiconductor devices as well as electronic devices employing such improved devices. (Page 1, lines 5-7.) In recent years, various wire-bond-type chip size packages (CSPs) have appeared in response to multi-electrode trends of semiconductor chips. (Page 1, lines 11-13.) The CSPs include flexible printed circuit (FPC) type CSPs and rigid substrate type CSPs. (Figs. 7A and 7B, respectively.)

The FPC-type CPS comprises a base **a** composed of a polyimide resin, and wiring films **b** composed of a metal such as copper formed on the surface of the base **a**. Holes **c** for forming electrodes are formed in the base **a**, and fine spherical electrodes **d** composed of solder are formed in the electrode-forming holes. (Page 1, lines 13-19.)

Since it is impossible to reduce the diameter of the electrode-forming holes **c** below 25  $\mu$ m, reduction in the array pitch between the hole-electrodes is limited. (Page 2, lines 21-23 and page 5, lines 21-24) Accordingly, the appearance of the electrode-forming holes and the spherical electrodes is inferior. (Page 2, lines 25 and 26.)

The rigid substrate-type CPS comprises a rigid wiring substrate **i** having holes **j** for forming electrodes, wiring films **k** formed on the rigid wiring substrate **i**, and wiring films **l**. (Page 2, lines 2-7.) It is difficult to reduce the diameter of the electrode-forming holes to 0.35 mm or less. (Page 3, lines 6-8.)

Appellant has discovered an improved semiconductor device comprising, *inter alia*, a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes, where *the electrode forming holes have a diameter of 22  $\mu$ m or less*. (Page 3, line 23, page 4, line 2 and page 5, lines 21-23.) It is only possible to produce such fine holes using a novel patterning process also described in the specification. (Page 5, lines 7-18.) The increased fineness of the electrode-forming holes in the claimed semiconductor devices is of great significance, because it provides for an increase in the array density of the holes. (Specification, page 5, line 25 - page 6, line 1.)

**ISSUES:**

(a) Whether claims 1, 2, 11, and 12 are unpatentable under 35 U.S.C. § 103(a) as obvious in light of U. S. Patent No. 5,976,912 ( the Fukutomi *et al.* patent).

(b) Whether claim 3 is unpatentable under 35 U.S.C. § 103(a) as obvious in light of a combination of the Fukutomi *et al.* patent and U. S. Patent No. 5,859,475 ( the Freyman *et al.* patent).

(c) Whether claims 4 and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious in light of a combination of the Fukutomi *et al.* patent and U. S. Patent No. 5,909,057 ( the McCormick *et al.* patent).

(d) Whether claim 5 is unpatentable under 35 U.S.C. § 103(a) as obvious in light of a combination of the Fukutomi *et al.* patent and U. S. Patent No. 5,708,567 ( the Shim *et al.* patent).

(e) Whether claims 14 and 15 are unpatentable under 35 U.S.C. § 103(a) as obvious in light of the Fukutomi *et al.* patent.

**GROUPING OF CLAIMS:**

For the purposes of this appeal, claims 1-5 and 11-15 stand or fall together.

**ARGUMENT**

(a) Claims 1, 2, 11, and 12 would not have been obvious under 35 U.S.C. § 103(a) in light of the Fukutomi *et al.* patent. As conceded by the Examiner, the Fukutomi *et al.* patent does not disclose semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. (Final Office Action, mailed Sept. 11, 2001, Detailed Action, page 3.) Nonetheless, the examiner argues:

It would have been obvious to one skilled in the art to form the electrode-forming holes with the claimed diameter, since such a modification would have involved a mere change in the size or the dimension of a component. A change in size or dimension is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1995 [sic]).

On the contrary, a reduction in the size of electrode holes is not “a mere change in the size or dimension of a component” absent a known method for making the electrode holes smaller.

The Fukutomi *et al.* patent does not disclose or suggest such a method. Instead, the process for making the electrode-forming holes described in the Fukutomi *et al.* patent is different than the process described in applicants' specification. For example, in preparing the semiconductor devices shown in Fig.'s 24 and 25 of the Fukutomi *et al.* patent the electrode-forming holes are formed using an excimer laser. (Col. 25, lines 44-46.) Alternatively, the Fukutomi *et al.* patent teaches that the holes can be formed by drilling or punching. (Col. 25, lines 48-52.) Nothing in the record suggests that such methods can be employed to produce holes having a diameter of to 0.22 or less. And as explained at page 5, lines 23-25, the lower limit of the diameter is 0.25 mm for a conventional FPC type, or 0.35 mm for a rigid substrate type CPS.

Thus, the Fukutomi *et al.* patent is not an enabling reference which would have made obvious the claimed invention. As stated by the Federal Circuit in *Rockwell International Corp. v. United States*, 47 USPQ2d 1027, 1032 (Fed. Cir. 1998), "In order to render a claimed apparatus or method obvious, the prior art must enable one skilled in the art to make and use the apparatus or method. [citation omitted]" In the context of a challenge to a patent's validity, the court explained, "Defendants had the burden to prove that combining these references would suggest to one of ordinary skill in the art how to perform the missing process step with a reasonable likelihood of success [citations omitted]." Here, the examiner has not met his burden and has not established that the Fukutomi *et al.* patent would have suggested to one of ordinary skill in the art how to form electrode-forming holes with a diameter of 0.22 mm or less. Therefore, the Fukutomi *et al.* patent would not have made obvious claims 1, 2, 11, and 12, so that the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

(b) Claim 3, a claim that additionally requires that a metal ring is bonded on a front surface of a base at the exterior of connection sections with wires in the wiring films, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the Freyman *et al.* patents. The Freyman *et al.* patent is relied upon merely because it teaches "a metal ring 31 being bonded on the front surface of the base 201 at the exterior of the connecting sections with wires 701 . . ." Nothing in the Freyman *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi

*et al.* and the Freyman *et al.* patents would not have made obvious claim 3, so that the rejection of this claim under 35 U.S.C. § 103(a) should be withdrawn.

(c) Claims 4 and 13, claims that additionally require that the semiconductor element and the wires are covered with a reinforcement having a downward indented face, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the McCormick *et al.* patents. The McCormick *et al.* patent is relied upon merely because it teaches, "a reinforcement 214 having a downward indented face covering the semiconductor element 200 . . ." Nothing in the McCormick *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi *et al.* and the McCormick *et al.* patents would not have made obvious claims 4 and 13, so that the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

(d) Claim 5, a claim that additionally requires that the base have vent holes, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the Shim *et al.* patents. The Shim *et al.* patent is relied upon merely because it teaches, a "base 20 having the vent holes 23 . . ." Nothing in the Shim *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi *et al.* and the Shim *et al.* patents would not have made obvious claim 5, so that the rejection of this claim under 35 U.S.C. § 103(a) should be withdrawn.

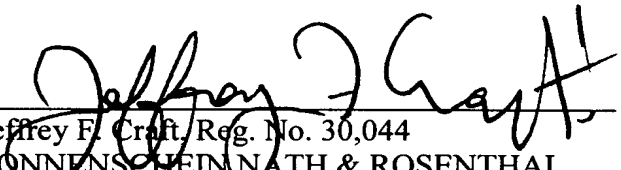
(e) Claims 14 and 15, the claims that additionally require that the wiring films are formed by a layer of copper covered by a nickel layer so that the wires are bonded to the nickel layer, would not have been obvious under 35 U.S.C. § 103(a) in light of the Fukutomi *et al.* patent. As discussed above, nothing in the Fukutomi *et al.* patent would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, the Fukutomi *et al.* and the Shim *et al.* patents would not have made obvious claims 14 and 15, so that the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

**CONCLUSION:**

For the foregoing reasons, claims 1-5 and 11-15, all the claims on appeal should be found allowable.

Respectfully submitted,

Date: July 11, 2002



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Attorneys for Appellant

**APPENDIX****CLAIMS ON APPEAL**

1. A semiconductor device comprising:
  - a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes;
  - a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base;
  - a semiconductor element positioned on said front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to said front surface of the base; and
  - wire for bonding the electrodes of the semiconductor element to the corresponding wiring films.
2. A semiconductor device according to claim 1, wherein said semiconductor element and said wires are sealed with a resin.
3. A semiconductor device according to claim 1, wherein a metal ring is bonded on the front surface of the base at the exterior of the connecting sections with wires in the wiring films.
4. A semiconductor device according to claim 1, wherein said semiconductor element and said wires are covered with a reinforcement having a downward indented face.
5. A semiconductor device according to any one of claims 1 to 4, wherein the base has vent holes.
11. An electronic device comprising a semiconductor device comprising: a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes; a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base; a semiconductor element positioned on said a front surface of the base with an insulating film therebetween, the back surface of the



semiconductor element being bonded to said front surface of the base; and wires for bonding the electrodes of the semiconductor element to the corresponding wiring films.

12. An electronic device according to claim 11, wherein said semiconductor element and said wires are sealed with a resin.

13. An electronic device according to claim 11, wherein said semiconductor element and said wires are covered with a reinforcement having a downward indented face.

14. An electronic device according to claim 11, wherein the wiring films comprise two layers with a layer of nickel covering the layer of copper so that the wires are connected to the nickel layer.

15. A semiconductor device comprising:

a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes;

a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base;

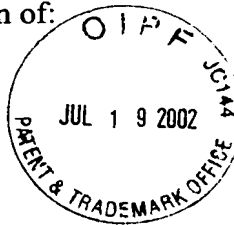
a semiconductor element positioned on said front surface of the base with an insulating film between, the back surface of the semiconductor element being bonded to said front surface of the base; and

wires for bonding the electrodes of the semiconductor element to the corresponding wiring films, the wiring films being formed by a layer of copper covered by a nickel layer so that the wires are bonded to the nickel layer.

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(b) Claim 3, a claim that additionally requires that a metal ring is bonded on a front surface of a base at the exterior of connection sections with wires in the wiring films, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the Freyman *et al.* patents. The Freyman *et al.* patent is relied upon merely because it teaches "a metal ring 31 being bonded on the front surface of the base 201 at the exterior of the connecting sections with wires 701 . . ." Nothing in the Freyman *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi

*et al.* and the Freyman *et al.* patents would not have made obvious claim 3, so that the rejection of this claim under 35 U.S.C. § 103(a) should be withdrawn.

(c) Claims 4 and 13, claims that additionally require that the semiconductor element and the wires are covered with a reinforcement having a downward indented face, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the McCormick *et al.* patents. The McCormick *et al.* patent is relied upon merely because it teaches, "a reinforcement 214 having a downward indented face covering the semiconductor element 200 . . ." Nothing in the McCormick *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi *et al.* and the McCormick *et al.* patents would not have made obvious claims 4 and 13, so that the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

(d) Claim 5, a claim that additionally requires that the base have vent holes, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the Shim *et al.* patents. The Shim *et al.* patent is relied upon merely because it teaches, a "base 20 having the vent holes 23 . . ." Nothing in the Shim *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi *et al.* and the Shim *et al.* patents would not have made obvious claim 5, so that the rejection of this claim under 35 U.S.C. § 103(a) should be withdrawn.

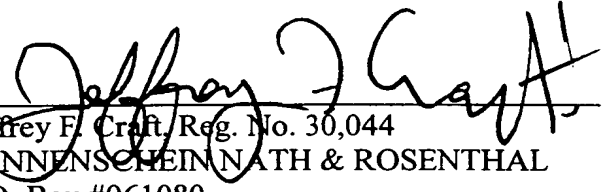
(e) Claims 14 and 15, the claims that additionally require that the wiring films are formed by a layer of copper covered by a nickel layer so that the wires are bonded to the nickel layer, would not have been obvious under 35 U.S.C. § 103(a) in light of the Fukutomi *et al.* patent. As discussed above, nothing in the Fukutomi *et al.* patent would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, the Fukutomi *et al.* and the Shim *et al.* patents would not have made obvious claims 14 and 15, so that the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

**CONCLUSION:**

For the foregoing reasons, claims 1-5 and 11-15, all the claims on appeal should be found allowable.

Respectfully submitted,

Date: July 11, 2002



\_\_\_\_\_  
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Attorneys for Appellant

**APPENDIX****CLAIMS ON APPEAL**

1. A semiconductor device comprising:  
a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes;  
a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base;  
a semiconductor element positioned on said front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to said front surface of the base; and  
wire for bonding the electrodes of the semiconductor element to the corresponding wiring films.
2. A semiconductor device according to claim 1, wherein said semiconductor element and said wires are sealed with a resin.
3. A semiconductor device according to claim 1, wherein a metal ring is bonded on the front surface of the base at the exterior of the connecting sections with wires in the wiring films.
4. A semiconductor device according to claim 1, wherein said semiconductor element and said wires are covered with a reinforcement having a downward indented face.
5. A semiconductor device according to any one of claims 1 to 4, wherein the base has vent holes.
11. An electronic device comprising a semiconductor device comprising: a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes; a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base; a semiconductor element positioned on said a front surface of the base with an insulating film therebetween, the back surface of the



semiconductor element being bonded to said front surface of the base; and wires for bonding the electrodes of the semiconductor element to the corresponding wiring films.

12. An electronic device according to claim 11, wherein said semiconductor element and said wires are sealed with a resin.

13. An electronic device according to claim 11, wherein said semiconductor element and said wires are covered with a reinforcement having a downward indented face.

14. An electronic device according to claim 11, wherein the wiring films comprise two layers with a layer of nickel covering the layer of copper so that the wires are connected to the nickel layer.

15. A semiconductor device comprising:

a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes;

a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base;

a semiconductor element positioned on said front surface of the base with an insulating film between, the back surface of the semiconductor element being bonded to said front surface of the base; and

wires for bonding the electrodes of the semiconductor element to the corresponding wiring films, the wiring films being formed by a layer of copper covered by a nickel layer so that the wires are bonded to the nickel layer.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re U.S. Patent Application of:  
Ohsawa *et al.*

Serial No.: 09/199,305

Filed: November 25, 1998

For: **A SEMICONDUCTOR DEVICE AND  
AN ELECTRICAL DEVICE USING  
THE SEMICONDUCTOR DEVICE**



Examiner: L. Thai

Group Art Unit: 2811

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**APPELLANT'S MAIN BRIEF ON APPEAL**

Assistant Commissioner for Patents  
Washington D.C. 20231

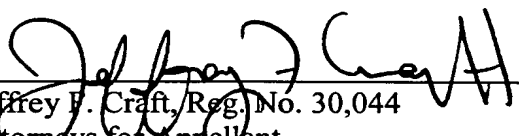
Sir:

Appellant is submitting herewith, in triplicate, Appellant's Main Brief on Appeal under 37 C.F.R. §1.192 in support of the Notice of Appeal filed on February 11, 2002.

The Commissioner is hereby authorized to charge any fee due not paid by check and to credit any overpayment in fees associated with this communication to Deposit Account No. 19-3140. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

SONNENSCHN NATH & ROSENTHAL

  
Jeffrey F. Craft, Reg. No. 30,044  
Attorneys for Appellant

I hereby certify that this original and two copies of this correspondence and any fee being referred to as attached or enclosed is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231 on July 11, 2002.

July 11, 2002  
Date

  
Kathleen Gaines

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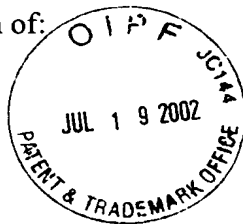
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**APPELLANT'S MAIN BRIEF ON APPEAL**

Assistant Commissioner for Patents

Washington D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. §1.192, Appellant herewith submits this Brief in support of the Appeal of the above-referenced application.

**REAL PARTY IN INTEREST:**

Sony Corporation, a Japanese corporation with offices at 7-35 Kitashinagawa 6-Chome, Shinagawa-Ku, Tokyo, Japan is the real party in interest.

**RELATED APPEALS AND INTERFERENCES:**

Neither Appellant, Appellant's legal representative, or its assignees are aware of any other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**STATUS OF CLAIMS:**

Claims 1-13 were present in the original application. Claims 6-10 were cancelled in response to a restriction requirement. Claims 14 and 15 were added by amendment. Appellant appeals final rejection of claims 1-5 and 11-15.

## STATUS OF AMENDMENTS:

No amendments were filed subsequent to final rejection

## SUMMARY OF THE INVENTION:

Appellant has discovered improved semiconductor devices as well as electronic devices employing such improved devices. (Page 1, lines 5-7.) In recent years, various wire-bond-type chip size packages (CSPs) have appeared in response to multi-electrode trends of semiconductor chips. (Page 1, lines 11-13.) The CSPs include flexible printed circuit (FPC) type CSPs and rigid substrate type CSPs. (Figs. 7A and 7B, respectively.)

The FPC-type CPS comprises a base **a** composed of a polyimide resin, and wiring films **b** composed of a metal such as copper formed on the surface of the base **a**. Holes **c** for forming electrodes are formed in the base **a**, and fine spherical electrodes **d** composed of solder are formed in the electrode-forming holes. (Page 1, lines 13-19.)

Since it is impossible to reduce the diameter of the electrode-forming holes **c** below 25 mm, reduction in the array pitch between the hole-electrodes is limited. (Page 2, lines 21-23 and page 5, lines 21-24) Accordingly, the appearance of the electrode-forming holes and the spherical electrodes is inferior. (Page 2, lines 25 and 26.)

The rigid substrate-type CPS comprises a rigid wiring substrate **i** having holes **j** for forming electrodes, wiring films **k** formed on the rigid wiring substrate **i**, and wiring films **l**. (Page 2, lines 2-7.) It is difficult to reduce the diameter of the electrode-forming holes to 0.35 mm or less. (Page 3, lines 6-8.)

Appellant has discovered an improved semiconductor device comprising, *inter alia*, a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes, where *the electrode forming holes have a diameter of 22 mm or less*. (Page 3, line 23, page 4, line 2 and page 5, lines 21-23.) It is only possible to produce such fine holes using a novel patterning process also described in the specification. (Page 5, lines 7-18.) The increased fineness of the electrode-forming holes in the claimed semiconductor devices is of great significance, because it provides for an increase in the array density of the holes. (Specification, page 5, line 25 - page 6, line 1.)

**ISSUES:**

(a) Whether claims 1, 2, 11, and 12 are unpatentable under 35 U.S.C. § 103(a) as obvious in light of U. S. Patent No. 5,976,912 ( the Fukutomi *et al.* patent).

(b) Whether claim 3 is unpatentable under 35 U.S.C. § 103(a) as obvious in light of a combination of the Fukutomi *et al.* patent and U. S. Patent No. 5,859,475 ( the Freyman *et al.* patent).

(c) Whether claims 4 and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious in light of a combination of the Fukutomi *et al.* patent and U. S. Patent No. 5,909,057 ( the McCormick *et al.* patent).

(d) Whether claim 5 is unpatentable under 35 U.S.C. § 103(a) as obvious in light of a combination of the Fukutomi *et al.* patent and U. S. Patent No. 5,708,567 ( the Shim *et al.* patent).

(e) Whether claims 14 and 15 are unpatentable under 35 U.S.C. § 103(a) as obvious in light of the Fukutomi *et al.* patent.

**GROUPING OF CLAIMS:**

For the purposes of this appeal, claims 1-5 and 11-15 stand or fall together.

**ARGUMENT**

(a) Claims 1, 2, 11, and 12 would not have been obvious under 35 U.S.C. § 103(a) in light of the Fukutomi *et al.* patent. As conceded by the Examiner, the Fukutomi *et al.* patent does not disclose semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. (Final Office Action, mailed Sept. 11, 2001, Detailed Action, page 3.) Nonetheless, the examiner argues:

It would have been obvious to one skilled in the art to form the electrode-forming holes with the claimed diameter, since such a modification would have involved a mere change in the size or the dimension of a component. A change in size or dimension is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1995 [sic]).

On the contrary, a reduction in the size of electrode holes is not “a mere change in the size or dimension of a component” absent a known method for making the electrode holes smaller.

The Fukutomi *et al.* patent does not disclose or suggest such a method. Instead, the process for making the electrode-forming holes described in the Fukutomi *et al.* patent is different than the process described in applicants' specification. For example, in preparing the semiconductor devices shown in Fig.'s 24 and 25 of the Fukutomi *et al.* patent the electrode-forming holes are formed using an excimer laser. (Col. 25, lines 44-46.) Alternatively, the Fukutomi *et al.* patent teaches that the holes can be formed by drilling or punching. (Col. 25, lines 48-52.) Nothing in the record suggests that such methods can be employed to produce holes having a diameter of to 0.22 or less. And as explained at page 5, lines 23-25, the lower limit of the diameter is 0.25 mm for a conventional FPC type, or 0.35 mm for a rigid substrate type CPS.

Thus, the Fukutomi *et al.* patent is not an enabling reference which would have made obvious the claimed invention. As stated by the Federal Circuit in *Rockwell International Corp. v. United States*, 47 USPQ2d 1027, 1032 (Fed. Cir. 1998), "In order to render a claimed apparatus or method obvious, the prior art must enable one skilled in the art to make and use the apparatus or method. [citation omitted]" In the context of a challenge to a patent's validity, the court explained, "Defendants had the burden to prove that combining these references would suggest to one of ordinary skill in the art how to perform the missing process step with a reasonable likelihood of success [citations omitted]." Here, the examiner has not met his burden and has not established that the Fukutomi *et al.* patent would have suggested to one of ordinary skill in the art how to form electrode-forming holes with a diameter of 0.22 mm or less. Therefore, the Fukutomi *et al.* patent would not have made obvious claims 1, 2, 11, and 12, so that the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

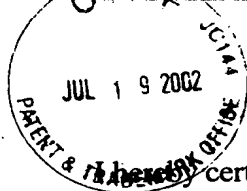
(b) Claim 3, a claim that additionally requires that a metal ring is bonded on a front surface of a base at the exterior of connection sections with wires in the wiring films, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the Freyman *et al.* patents. The Freyman *et al.* patent is relied upon merely because it teaches "a metal ring 31 being bonded on the front surface of the base 201 at the exterior of the connecting sections with wires 701 . . ." Nothing in the Freyman *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi

*et al.* and the Freyman *et al.* patents would not have made obvious claim 3, so that the rejection of this claim under 35 U.S.C. § 103(a) should be withdrawn.

(c) Claims 4 and 13, claims that additionally require that the semiconductor element and the wires are covered with a reinforcement having a downward indented face, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the McCormick *et al.* patents. The McCormick *et al.* patent is relied upon merely because it teaches, "a reinforcement 214 having a downward indented face covering the semiconductor element 200 . . ." Nothing in the McCormick *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi *et al.* and the McCormick *et al.* patents would not have made obvious claims 4 and 13, so that the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

(d) Claim 5, a claim that additionally requires that the base have vent holes, would not have been obvious under 35 U.S.C. § 103(a) in light of a combination of the Fukutomi *et al.* and the Shim *et al.* patents. The Shim *et al.* patent is relied upon merely because it teaches, a "base 20 having the vent holes 23 . . ." Nothing in the Shim *et al.* patent, whether considered alone or whether considered in combination with the Fukutomi *et al.* patent, would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, a combination of the Fukutomi *et al.* and the Shim *et al.* patents would not have made obvious claim 5, so that the rejection of this claim under 35 U.S.C. § 103(a) should be withdrawn.

(e) Claims 14 and 15, the claims that additionally require that the wiring films are formed by a layer of copper covered by a nickel layer so that the wires are bonded to the nickel layer, would not have been obvious under 35 U.S.C. § 103(a) in light of the Fukutomi *et al.* patent. As discussed above, nothing in the Fukutomi *et al.* patent would have suggested the claimed semiconductor devices having electrode-forming holes with a diameter of 0.22 mm or less. Therefore, the Fukutomi *et al.* and the Shim *et al.* patents would not have made obvious claims 14 and 15, so that the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.



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Kathleen Gaines

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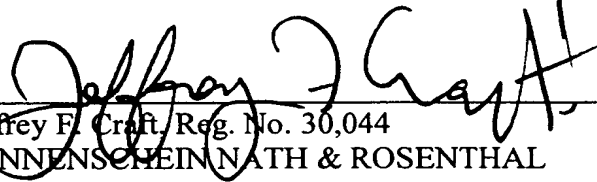


**CONCLUSION:**

For the foregoing reasons, claims 1-5 and 11-15, all the claims on appeal should be found allowable.

Respectfully submitted,

Date: July 11, 2002

  
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**APPENDIX****CLAIMS ON APPEAL**

1. A semiconductor device comprising:
  - a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes;
  - a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base;
  - a semiconductor element positioned on said front surface of the base with an insulating film therebetween, the back surface of the semiconductor element being bonded to said front surface of the base; and
  - wire for bonding the electrodes of the semiconductor element to the corresponding wiring films.
2. A semiconductor device according to claim 1, wherein said semiconductor element and said wires are sealed with a resin.
3. A semiconductor device according to claim 1, wherein a metal ring is bonded on the front surface of the base at the exterior of the connecting sections with wires in the wiring films.
4. A semiconductor device according to claim 1, wherein said semiconductor element and said wires are covered with a reinforcement having a downward indented face.
5. A semiconductor device according to any one of claims 1 to 4, wherein the base has vent holes.
11. An electronic device comprising a semiconductor device comprising: a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes; a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base; a semiconductor element positioned on said a front surface of the base with an insulating film therebetween, the back surface of the

semiconductor element being bonded to said front surface of the base; and wires for bonding the electrodes of the semiconductor element to the corresponding wiring films.

12. An electronic device according to claim 11, wherein said semiconductor element and said wires are sealed with a resin.

13. An electronic device according to claim 11, wherein said semiconductor element and said wires are covered with a reinforcement having a downward indented face.

14. An electronic device according to claim 11, wherein the wiring films comprise two layers with a layer of nickel covering the layer of copper so that the wires are connected to the nickel layer.

15. A semiconductor device comprising:

a plurality of wiring films formed on a front surface of a base comprising an insulating resin and having electrode-forming holes with a diameter of 22 mm or less, the surfaces of the wiring films and the surface of the base being positioned on the same plane and at least parts of the wiring films overlapping with the electrode-forming holes;

a conductive material embedded into the electrode-forming holes to form external electrodes on the back surface, away from the wiring films, of the base;

a semiconductor element positioned on said front surface of the base with an insulating film between, the back surface of the semiconductor element being bonded to said front surface of the base; and

wires for bonding the electrodes of the semiconductor element to the corresponding wiring films, the wiring films being formed by a layer of copper covered by a nickel layer so that the wires are bonded to the nickel layer.